IMPLEMENTATION OF SYNCHRONIZATION FOR 2X2 MIMO WLAN SYSTEMS

Hsin-Lei Lin, Chia-Chen Hsu, Robert C. Chang

Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan

ABSTRACT

The proposed synchronization is designed for 2x2 MIMO OFDM WLAN systems. A novel CSIO structure is implemented to recover the carrier frequency. The proposed design chiefly improves the conventional CORDIC-based structure which is used at each accumulated phase. Considering the iterative CORDIC computation, our CSIO structure only operates the CORDIC once. Moreover, the timing controller negotiates these two antenna input signals and gates the useless signal to reduce the power consumption. This architecture is simulated by UMC 0.18 μm 1P6M CMOS technology, and the CSIO function is also emulated by VirtexII XC2V1500. It provides the high precision with the area of 1.682 mm². The power consumption is 90.53 mW at 20MHz.

I. INTRODUCTION

The OFDM system plays an important role to cope with the multipath channel in IEEE 802.11a/g/n WLAN system. The synchronization of 2x2 MIMO WLAN systems is shown in Fig. 1. The novel CORDIC-based Sinusoid Iteration Oscillator (CSIO), division sharing, and the timing controller are proposed for synchronization. In the MIMO OFDM system, the preamble is used for detecting the frame and diminishing the effect of channel and carrier frequency offset. However, it results in sensitive frequency. The proposed design deals with the timing and carrier synchronization efficiently.

There are several ways to achieve the carrier synchronization. Most synchronization techniques use DSP processor, but cost a lot of power consumption. For hardware implementation, instead of using the sin/cos table [1] to control the digital oscillator, Zou et al. use the CORDIC algorithm to avoid the inaccuracy of the table and use the memory efficiently [2]. Considering the iterative CORDIC computation, our CSIO structure only operates the CORDIC once. Our proposed structure of 2x2 MIMO WLAN systems improves the performance of precision and stable oscillation in real time by CSIO. The purpose of our idea is to reduce the CORDIC operating frequency in each accumulated phase.

II. THE NOVEL CSIO SYNCHRONIZATION ARCHITECTURE

The proposed synchronization architecture consists of timing and carrier frequency synchronization as shown in Fig. 1. The first part detects the signal frame boundary and starts up the timing controller while we receive the short preambles. Then the frequency offset is measured by the ML algorithm when the long preambles received. The operation of the novel CSIO construction via a CORDIC calculation and the cascaded sinusoid iteration recovers the frequency offset by coarse and fine carrier synchronization.

A. The cross-correlation for timing synchronization

Since the cross-correlation [3] is correlated with a given sequence, we can regard it as a match filter with the sixteen taps. These known complex sequences are floating point numbers that cost a lot of hardware to be transformed into fixed point numbers. We quantify the coefficient sequence by three levels, 0, 1, and -1 [4] without using multipliers, since the peak is obtained validly by the quantified coefficients in every sixteen samples. The cross-correlation peak is produced to start the timing synchronization controller and recognize the coarse preamble boundary.

B. Frequency synchronization

The short and long preambles are used for the coarse and fine carrier frequency synchronization respectively as given Fig. 2. The maximum likelihood value is found by picking up the maximum in the sequential autocorrelation value. In the short training sequence, the correlator accumulates 16 samples, and then we obtain the rotated phase per sample by shifting 4 bits. We assume that if the radian of the rotated phase is smaller than 0.5, the rotated angle is similar to tangent of the angle. The real axis value divided by the imaginary axis value is the rotated phase under this hypothesis. We turn off the autocorrelation of the short preamble while the coarse carrier synchronization accomplishes. The four times precision frequency estimation which uses the long preambles is switched on by the boundary detection. The fine carrier synchronized structure is similar to the coarse one but with 64 taps correlation and 6-bit shift output values.

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The novel CSIO structure for the synchronization

The CORDIC structure is used for rotating the vector of frequency offset as the front end of the CSIO shown in Fig. 3. We suppose the initial vector is on the real axis. It means that the real axis signal $X_0$ is equal to one, and the imaginary axis signal $Y_0$ equals to zero. The coefficient $K$ is given by different rotative situations. The auxiliary computing angle $Z_0$ is phase rotation that could be estimated by the autocorrelation. The stage controller is affected by the signal $Z_{out}$, and it controls the shifts and $\tan^{-1}$ table.

The sinusoid iteration oscillator deduces from the trigonometric function. The trigonometric function as in (1) is utilized to calculate the values of $\sin(k\theta)$ and $\cos(k\theta)$, where $k=1, 2, 3 ... N_T$ and $N_T$ is the number of the receiver signals.

$$\sin(A + B) = \sin A \cos B + \cos A \sin B$$

$$\cos(A + B) = \cos A \cos B - \sin A \sin B$$

In order to address the iterative scheme, we assume that $A = \theta$ and $B = \theta$, $2\theta$, $3\theta$, ..., $(k-1)\theta$. The first rotated vector, $\sin \theta$ and $\cos \theta$, can be computed by the CORDIC, and we take it for the initial value of the SIO as in (2).

$$\sin(\theta + B) = \sin \theta \cos B + \cos \theta \sin B$$

$$\cos(\theta + B) = \cos \theta \cos B - \sin \theta \sin B$$

The oscillator architecture in Fig. 3 receives the real and imaginary signals from the CORDIC structure. The stage controller starts the modified oscillation and controls the iteration feedback computing. The last frequency rotated vectors $(S(i) \cdot C(i))$ and the initial phase offset $(S(0) \cdot C(0))$.

### III. Implementation and comparison results

Assume that the communicated channel is affected by AWGN, signal delay, and frequency offset. In the test bench, the SNR is set to 25dB, and the frequency offset are 600 kHz and 300 kHz at the antenna 1 and the antenna 2, respectively. The cross-correlation and the autocorrelation synchronize the timing and find the coarse rotated phase as Fig. 4(a). The proposed 2x2 MIMO WLAN synchronization can cope with the different frequency rotations at each antenna. Fig. 4(b) proves that the design is successful in 600 kHz and 300 kHz rotation.

The synchronization architecture of wireless systems was implemented using 0.18 $\mu$m 1P6M CMOS technology at 1.8V. Table 1 shows the comparison between our proposed CSIO structure and other circuits for wireless system. For the WLAN system, the symbol clock frequency tolerance shall be 40 ppm and the maximum length is 4095, that the frequency tolerant range can be derived between 200 kHz and 407 Hz. It also compares the specification of the single and 2x2 MIMO WLAM systems with 20 MHz operation frequency. The wordlength is 16-bit complex number input and output signal which can describe the value of the fine carrier synchronization to avoid the quantified error. The core area is about 1.682 mm$^2$ without doubling the area and power of the single antenna system shown in table 2.

### IV. CONCLUSION

In this paper, the novel CSIO architecture efficiently reduced hardware is proposed for wireless systems with training sequence. The Sinusoid Iteration Oscillator (SIO) is instead of the conventional phase accumulator before the CORDIC circuit. This architecture was implemented and verified using UMC 0.18 $\mu$m 1P6M CMOS technology at 1.8V, for the 600 kHz and 300 kHz frequency offsets in an AWGN wireless system. It provides not only the high precision, but also a small area of 1.682 mm$^2$ in area and low power consumption of 90.53 mW.

### REFERENCES


