A Novel Start-Controlled Phase/Frequency Detector for
Multiphase-Output Delay-Locked Loops

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Abstract—In this paper, a novel start-controlled phase/frequency detector (PFD) for multiphase-output delay-locked loops (MODLLs) is presented. In the proposed PFD, the start-controlled circuit is used to provide a precise multiphase-output without the locking problem. The PFD utilizes a new NAND-resetable dynamic DFF so that a shorter reset path is achieved. Thus, lower power consumption and higher speed can be obtained. A MODLL using the proposed start-controlled PFD is post-layout simulated using the TSMC 0.35- μm 2P4M CMOS process. The results show that the total delay time between the input and the output of the MODLL is just one clock cycle and all of the delay cells provide precise multiphase-output without false locking or harmonic locking. Compared to the static DFF based start-controlled PFD, the power consumption of the proposed NAND-resetable dynamic DFF based PFD is reduced at least 61%. The power consumption of the proposed start-controlled PFD is 100 μW at 2V and 100MHz. The area of the MODLL circuit is 426 μm × 381 μm.

Index Terms—Delay-locked loop, multiphase-output, resetable D-flip-flop, start-controlled circuit, locking problem.

I. INTRODUCTION

With the evolution and continuing scaling of CMOS technologies, the demand for high-speed and high-integration density VLSI systems has recently grown exponentially. However, the synchronization problem between chip modules is serious and becoming one of the bottlenecks for high-performance systems. Many approaches exist for dealing with clock synchronization. Phase-locked loops (PLLs) [1,2] and delay-locked loops (DLLs) [3-6] are widely employed for the purpose of clock synchronization. Meanwhile, the jitter performance of DLLs is superior to that of PLLs.

In many DLLs applications, such as timing recovery [7,8] and frequency multiplier [9,10], the multiphase-output of voltage-controlled delay line (VCDL) is used to implement the circuit function. In these cases, the total delay time between input and output of the MODLL is needed to just one clock cycle. However, conventional DLL may suffer from the locking problem over a wide operating range [5]. In this paper, a start-controlled PFD is proposed to fix this problem so that the total delay time from all delay stages is precisely one clock cycle of the input reference signal.

The locking problem of conventional DLLs will be discussed in Section II. In Section III, the architecture of the proposed start-controlled PFD is presented. Section IV describes the design of the MODLL. The post-layout simulation results and comparisons are given in Section V. Section VI concludes this paper with a summary.

![Fig. 1. Block diagram of the conventional DLL.](image)

II. LOCKING PROBLEM OF CONVENTIONAL DLLS

A conventional DLL, as shown in Fig. 1, consists of the phase detector (PD), the charge-pump (CP), the loop filter, and the VCDL. In the DLL, the reference clock, ref_clk, is propagated through the VCDL. The output signal, out_clk, at the end of the delay line is compared with the reference signal. If the time delay is different from integer multiples of clock periods, the closed loop will automatically correct it by changing the delay time of the delay line through the control signal, Vcnt, of the loop filter. Assume that the maximum and the minimum delay of the VCDL are TVCDLVCDL TMaxVCDL and TVCDLVCDL TMinVCDL, respectively. As a result, the period of the input signal should satisfy the following inequality:

$$\text{Min}(TV_{\text{CDL_min}}, 2 \times TV_{\text{CDL_min}}) < T_{\text{CLK}} < \text{Max}(2, 3) \times TV_{\text{CDL_min}}$$

(1)

Equation (1) shows that the DLL is prone to the false locking problem when process variations are taken into account [5]. Therefore, some solutions [4-6, 9-11] were proposed to overcome the locking problem. They are described as follows.

First, the basic idea is to use a PFD [3]. The PFD has a capture range of ±π which is wider than ±π of the phase detector. Thus, the PFD is a better choice for the wide range operation. However, the PFD can’t be used in the DLL alone without any control circuit because the DLL will try to lock a zero delay. Therefore, a PFD combined with a control circuit was reported in [4]. Nevertheless, in some cases, especially for high-frequency operations, the initial delay between ref_clk and out_clk may be larger than two clock cycles and harmonic locking would occur [6].

Secondly, an all-analog DLL using a replica delay line [5] has been developed to solve the locking problem of a conventional DLL. If the delay range of the VCDL satisfies the relation TV_{\text{CDL_min}} < TV_{\text{CDL_max}} / 7, the DLL will have a maximum operation range of 7:1. However, due to EX-NOR as PD used in replica delay line, the duty cycle of input signal must be exactly equal to 50%. The design efforts must increase especially for
charge pump in which the pull-up current is not equal to pull-down current. 

Thirdly, a self-correcting technique for a digital-controlled DLL is presented in [9]. The locking problem is solved by the addition of a lock-detect circuit and the modified phase detector. Although this self-correcting DLL avoids false locking, the outputs of the VCDL are required to have an exact 50% duty cycle.

A PD with a reset circuitry was used to overcome the locking problem [10]. However, when the initial delay between the input and the output is larger than two clock cycles, the locking problem exists yet. A DLL using a stage selector was designed for fast-locked and wide-range operations, but it requires an additional VCDL, which increases the area [11]. The DLL developed in [6] uses a start-controlled circuit to avoid the locking problem. Its basic idea is similar to [4] and it takes the harmonic locking situation stated above into account. But the architecture of the start-controlled circuit is more complicated than [4] so that the circuit area and the power consumption will be increased.

Therefore, a resettable dynamic DFF based start-controlled PFD for the MODLL is proposed in this paper. It can be used to solve the locking problem and the duty cycle is not necessary to be exactly 50%.

III. START-CONTROLLED PFD

The circuit architecture of the start-controlled PFD is modified from Kim’s [4] and its operation principle is the same to Chang’s [6]. First, the delay between input and output of the VCDL is initially set to the minimum value and then allows the down signal of the PFD output activated, supposing that the VCDL’s delay increases with the control voltage decreasing. Therefore, the delay between input and output of the VCDL will increase until it reaches one clock cycle of the input signal. Thus, the DLL will not fall into false locking and the latency is fixed to one clock cycle no matter how long a delay the VCDL provides.

The block diagram and the resettable static DFF of the modified start-controlled PFD are shown in Fig. 3. It is composed of only three rising-edge triggered static DFFs and two static NAND gates. Compared to Kim’s, the Rdy is added to initialize the delay of the VCDL. The timing diagram of the modified start-controlled PFD is shown in Fig. 4. Initially, the start signal is set to low in order to clear the three outputs of the DFFs. Therefore, Rdy is low and pulls the control voltage to Vref, i.e., sets the VCDL delay to its minimum value. In this way, the two inputs of the PFD are at the low level. When the start signal goes to high, the Rdy signal will also go to high after the rising edge of ref_clk. So, the first rising edge of ref_clk can be virtually hidden and neglected during phase comparison. The delay of VCDL will increase until it is equal to one clock cycle of the input signal due to the nature of the negative feedback architecture. Since the start-controlled circuit forces the delay of the VCDL to its minimum value and controls the delay of the VCDL to increase until its delay is equal to one clock cycle, the DLL will not fall into false locking or harmonic locking.

Furthermore, the operating frequency of the modified start-controlled PFD is limited because the resettable DFFs are static type. The static PFD is an asynchronous state machine. The delay time to reset all internal nodes determines the circuit speed. The reset path of the resettable static DFF is shown in the dash line in Fig. 3(b). The reset path forms a feedback path with nine gate delays. The dead-zone occurs when the loop is in a lock mode and the output of the charge pump does not change for small changes in the input signals at the PFD. Any delay of the reset path causes dead-zone, which directly translates to jitter performance in the DLL and must be avoided [12]. To overcome the speed limitation and to reduce the reset path, the resettable static DFFs should be replaced by resettable dynamic DFFs and the PFD’s reset path must be shortened. In 1989, the dynamic true single phase clocking (TSPC) DFF was proposed by Yuan and Svensson in [13]. Although the DFF in [13] have higher operating frequency and a simple circuit structure, the DFF without reset-mode can’t be used in our design. Thus, a novel start-controlled PFD using the resettable dynamic DFF and the NAND-resetable dynamic DFF is proposed, as shown in Fig. 5. The proposed start-controlled circuit and the proposed PFD are composed of one resettable dynamic DFF and two NAND-resetable dynamic DFFs, respectively. Compared to [13], the M80 of Fig. 5(b) is added for the DFF to be resettable and the M80 ~ M93 of Fig. 5(c) are added for the DFF to be NAND-resetable. In Fig. 5(c), an inverter chain is used to eliminate the region of low gain near delay locked. The inverter chain is composed of three cascaded inverters. The elimination of the dead-zone is accomplished by producing an “up” current pulse and a “down” current pulse during each cycle. Therefore, both currents are of equal amplitude and width, the net effect on the output voltage of the charge pump circuit is zero [14, 15]. As a result, the number of transistors in the proposed start-controlled PFD circuit is reduced from 120 to 52 and the gate delay of the reset path is also reduced from 9 to 5.

In order to get equal delay between ref_clk and out_clk, a
dummy load should be added to the `out_clk` terminal. In addition, the duty cycle of `ref_clk` and `out_clk` is not necessary to be exact 50% because the DFFs are edge-trigger type. In comparison with Kim’s, this start-controlled PFD has the following advantages: the proposed circuit is simple, the operating frequency is higher, the reset path is shorter, the power is lower, and the duty cycle of `ref_clk` and `out_clk` is not required to be exactly 50%.

![Phase/Frequency Detector](image)

**Fig. 5.** Proposed start-controlled PFD. (a) Block diagram. (b) Resetable dynamic DFF. (c) NAND-resetable dynamic DFF.

**Fig. 6.** MODLL architecture.

**IV. MODLL DESIGN**

A MODLL has been designed using the start-controlled PFD presented above. The architecture of the MODLL is shown in Fig. 6. Compared with the conventional DLL, shown in Fig. 1, the PD is replaced by the proposed start-controlled PFD to avoid the locking problem and a PMOS is used to minimize the initial delay of VCDL. The voltage-controlled delay cell and its bias circuit are similar to those in [16] and [17], respectively. The delay cell consists of two cascaded current-steering inverters, and every two cascaded delay cells provide the quadrature output, `ck090` ~ `ck360`. In addition, two dummy delay cells are utilized to equalize the signal traces, `ck000` and `ck360`. Also, the dummy should be added to the output of the cascaded delay cells for the same reason. The open-drain inverting buffers are used to drive the capacitive loading for testing purposes. To provide an almost full-swing clock signal, the preamplifier and the buffers are added to the inputs of the VCDL and the start-controlled PFD, respectively.

![Layout of the MODLL](image)

**Fig. 7.** Layout of the MODLL.

![Post-layout simulation results](image)

**Fig. 8.** Post-layout simulation results. (a) Initial-state. (b) Locked-state. (c) Locking process of the control voltage.
IV. SIMULATION RESULTS AND COMPARISONS

The MODLL using the proposed start-controlled PFD has been post-layout simulated using the TSMC 0.35-μm 2P4M CMOS process. Fig. 7 shows the layout of the MODLL, whose active area is 426 μm x 381 μm. The post-layout simulation results with the reference frequency of 100MHz are shown in Fig. 8. Initially, the control voltage of the VCDL is set to VDD so that the initial delay of the VCDL is minimized. When the MODLL is locked, the multiphase-output clocks (ck600 ~ ck360) can be obtained. The proposed start-controlled PFD using the NAND-resetable dynamic DFF can provide multiphase-output clocks when process variation is taken into account. The locking time of the MODLL is less than 14 μs. In Fig. 9, the power consumption and the speed of the proposed, Kim’s, and Chang’s are compared. At 100MHz, the results show that the power consumption of the proposed start-controlled PFD is reduced at least 61% of Kim’s and 53% of Chang’s. At the same power consumption, 200 μW, the proposed start-controlled PFD, Kim’s and Chang’s can operate at 200MHz, 78MHz, and 92MHz, respectively. The maximum operating frequency of the proposed start-controlled PFD is up to 675MHz, whose power consumption is 616 μW. Table I shows the comparison results of the various techniques for the locking problem avoiding. The performance summary of the MODLL is show in Table II.

![Fig. 9. Comparison of power consumption and speed.](image)

Table I. Comparisons of various techniques

<table>
<thead>
<tr>
<th>Method</th>
<th>Extra hardware</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed start-controlled PFD</td>
<td>1 DFF (total 52 MOS including PFD)</td>
<td>Dynamic DFF, shorter reset path, lower power, smaller area, higher speed</td>
</tr>
<tr>
<td>[4] Static DFF based PFD with control circuit</td>
<td>1 DFF, some logic gates (total 120 MOS including static PFD)</td>
<td>Static DFF, higher reset path, higher power, lower speed, larger area</td>
</tr>
<tr>
<td>[5] Replica delay line</td>
<td>1 delay cell, current-steering, higher-order loop filter</td>
<td>Larger area, duty cycle of the signal must be 50%</td>
</tr>
<tr>
<td>[6] Start-controlled circuit</td>
<td>2 DFF, some logic gates (total 104 MOS including dynamic PFD)</td>
<td>Static DFF, larger area</td>
</tr>
<tr>
<td>[7] Selfcorrecting</td>
<td>Lock detector</td>
<td>Larger area, duty cycle of the signal must be 50%</td>
</tr>
<tr>
<td>[10] PD with reed oscillator</td>
<td>8 MOS</td>
<td>Static DFF, higher reset path, lower speed</td>
</tr>
<tr>
<td>[11] Stage selector</td>
<td>1 VCDL</td>
<td>Larger area</td>
</tr>
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</table>

Table II. Summary of the MODLL

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC 0.35-μm 2P4M CMOS</th>
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</thead>
<tbody>
<tr>
<td>Supply voltage</td>
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<tr>
<td>Operating frequency</td>
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<tr>
<td>VCDL gain</td>
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<tr>
<td>Pumping current</td>
<td>100 μA</td>
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<tr>
<td>Loop capacitance</td>
<td>&gt; 55 pF</td>
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<tr>
<td>Loop bandwidth</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Locking time</td>
<td>&lt; 14 μs</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 4 mW at 100 MHz</td>
</tr>
</tbody>
</table>

VI. CONCLUSIONS

In this paper, a novel start-controlled PFD for the MODLL is proposed. The total delay time between the input and the output of the MODLL is just one clock cycle and all of the delay cells provide precise multiphase-output without false locking or harmonic locking. The extra hardware of the MODLL is the start-controlled circuit, which is composed of only one proposed resetable dynamic DFF, which consists of 12 transistors. The start-controlled PFD has the following advantages: the proposed circuit is simple, the operating frequency is higher, the reset path is shorter, the power is lower, and the duty cycle of ref clk and out clk is not required to be exactly 50%. The proposed start-controlled PFD and the resetable dynamic DFF can be widely used in all of the analog DLLs and the low-power high-performance digital circuits and systems, respectively.

ACKNOWLEDGMENT

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REFERENCES